IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Shinichiroh IKEMASU, et al.

Group Art Unit: 2814

Serial No.: 10/050,169

Examiner: WEISS, Howard

Filed: January 18, 2002

Confirmation No.: 9818

For: HIGHLY INTEGRATED AND RELIABLE DRAM AND ITS MANUFACTURE

<u>PURSUANT TO 37 CFR 1.97(b)(4)</u>

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

March 19, 2004

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. The documents were made of record in related application Serial No. 10/166,620, filed June 12, 2002.

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. See 37 CFR 1.104(a) concerning the PTO duty to consider and use any such information. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.



The Commissioner is authorized to charge our Deposit Account No. 50-2866 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Stephen G. Adrian Attorney for Applicant(s) Reg. No. 32,878

SGA/arf

Enclosures: PTO-1449 and 18 References

Attorney Docket No.970607B

Suite 700 1250 Connecticut Avenue, N.W. Washington, D.C. 20036 Telephone: (202) 822-1100 INFORMATION DISCLOSURE CITATION PTO-1449 Atty. Docket No. 970607B

Serial No. 10/050,169

Applicant(s): Shinichiroh IKEMASU et al.

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U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
	AA	5,605,857	Jost et al.	02/97			
	AB	5,324,681	Lowrey et al.	06/94			
	AC_	5,292,677	Dennison	03/94			
	AD	5,281,549	Fazan et al.	01/94			
	AE	5,760,429	Yano et al.	6/98			
	AF	5,479,054	Tottori	12/95			
	AG	5,150,278	Gonzallez et al.	9/92			
	AH						
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OTHER DOCUMENTS

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	AQ	B.M. SOMERO et al.; "A Modular in-situ Integration Scheme for Deep Submicron", Proceedings of 10 th International VMIC; pages 28-34; June 1993.
	AR	M.F. CHISHOLM et al.; "A High Performance 0.5 um Five-Level Metal Process with Extendibility of Sub-Half Micron"; pages 22-28; June 1994.
	AS	M. RUTTEN et al.; "Pattern Density Effects in Tungsten CMP", Proceedings of 12 th International VMIC; pages 491-497; June 1995.
	АТ	I. NAIKI et al.; "Center Wordline Cell: A New Symmetric Layout Cell for 64Mb SRAM"; Technical Digest of IEDM; pages 817-820; December 1993.
	AU	T. KAGA et al.; "A 0.29-um2 MIM-Crown Cell and Process Technologies for 1-Gigabit DRAMs"; Technical Digest of IEDM; pages 927-929; December 1994.
	AV	H.K. KANG et al.; "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1 Gbit DRAMs"; Technical Digest of IEDM; pages 635-638; December 1994.
	A W	Y. OHJI et al.; "Ta ₂ O ₅ Capacitors Dielectric Material for Giga-bit DRAMs"; Technical Digest of IEDM; pages 111-114; December 1995.
	A X	Y. NISHIOKA et al.; "Giga-bit Scale DRAM Cell with New Simple Ru/(Ba,Sr)TiO3/Ru Stacked Capacitors Using X-ray Lithography"; Technical Digest of IEDM; pages 903-906; December 1995.
	AY	K.P. LEE et al.; "A Process Technology for 1 Giga-bit DRAM"; Technical Digest of IEDM; pages 907-910; December 1995.
	AZ	J.K. PARK et al.; "Isolation Merged Bit Line Cell(IMBC) for 1Gb DRAM and Beyond". Technical Digest of IEDM; pages 911-914; December 1995.
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